DEEN DAYAL UPADHYAYA COLLEGE

(University of Delhi)

Organizes

Fifth Hands-on Workshop

On

सत्यमेव जयते
DEPARTMENT OF BIOTECHNOLOGY
GOVERNMENT OF INDIA

VHDL Programming & Digital Circuit Designing with Implementation on FPGA

Under the Aegis of DBT Star College Program, ELECTRONICS

from

October 03 – 06, 2018

In collaboration with

CoreEL Technologies

Venue: Electronics Lab, Room No. 116 and 117, First Floor
Deen Dayal Upadhyaya College, New Delhi, Sector-3, Dwarka, New Delhi – 110078

About this Workshop : Knowledge, imagination and scientific methods are propelling our world to new heights and have made legacy hardware (circuit boards) obsolete. FPGAs are the new innovation when it comes to designing, integrating, and simulating systems. With unprecedented logic density increase and a host of other features, FPGAs are a compelling proposition for almost any type of design. Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. They can be reprogrammed to desired application after manufacturing and thus enable higher degrees of flexibility, faster time-to-market, and lower overall costs. They find applications in areas such as industrial imaging, surveillance, automation, Aerospace and Communications, etc.
Hardware Descriptive Language (HDL) or as a schematic design is used to design the behavior of FPGA. HDL form is more suited to work with large structures as it's possible to specify them functionally rather than having to draw every component. However, schematic entry allows for easier visualization of a design.

CoreEL : CoreEL Technologies is a one stop source for advanced tools, solutions, training and consultancy in VLSI and Embedded System technologies. They have been strategic partners to the Indian academia for over a decade now. Their area spans Product Sales & Support, consultancy, FDP and Student Programs across multiple disciplines. **CoreEL Technologies is the Sole Authorized Partner of Xilinx University Program (XUP) in India**.

Skills Gained After Completing this Workshop : Participants will have hands on experience on **NEXYS 4DDR FPGA** Boards from ***Xilinx*** and will be able to:

- Describe the coding techniques to configure the FPGA for an application
- Describe the general Artix-7 All Programmable FPGA architecture
- Understand the ISE and Vivado design flow
- Create and debug HDL designs
- Configure FPGA and verify hardware operation
- Configure FPGA architecture features, such as Clock Manager, using the Architecture Wizard
- Pinpoint design bottlenecks using the reports
- Utilize synthesis options to improve performance
- Create and integrate IP cores into design flow using IP Catalog
- Use Logic Analyzer to perform on-chip verification
- Perform simulation verification

Organizing Committee

Dr. Poonam Kasturi
Convener-DBT Star College (Electronics)
Associate Professor, Dept. of Electronics, DDUC
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Dr. Manoj Saxena
Coordinator-DBT Star College Program
Associate Professor, Dept. of Electronics, DDUC
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For any further Details Kindly contact

Dr. Manoj Saxena, *(*09968393104*) Room No. 114, First Floor,* Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, New Delhi 110078, Azad Hind Fauz Road, Sector-3, Dwarka (Nearest Metro Station: Dwarka Mor.)

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REGISTRATION FORM

(Kindly fill separate form for each Participant)

Name (In Block Letters) : _____

Gender : Male ☐ Female ☐

Category : Student ☐ Faculty ☐ ***Mobile No:*** _____

Complete Affiliation (College/ Institute and University:)	
Course *(For Students Only)*:	
Department *(For Faculty Members Only):*	
Email - address (Mandatory):	

Total number of seats : 40 *(To be filled on first-cum-first serve basis)*
All interested have to pre-register for the workshop. **No on the Spot Registration**

Registration Fees **(to be deposited in Cash) - Rs 200/-**

How to Apply: Interested participants should submit the duly filled form and fees (in cash) to Dr. Manoj Saxena, Coordinator-DBT Star College Program/Dr. Poonam Kasturi, Convener-Workshop/ latest by **October 02, 2018.** Participants have to make their own arrangements of local travel and stay. No expenses shall be reimbursed by the organizers.

Signature of the Delegate (with name)

Acknowledgment Slip for the Delegate

Received with thanks a sum of Rs. _____ from _____(*Name of the Delegate*) of _____(Course/ Department with Name of the Institute) towards registration fee for attending **4 Days Hands-on Workshop on "VHDL Programming & Digital Circuit Designing with Implementation on FPGA" by** Deen Dayal Upadhyaya College University of Delhi *Under the Aegis of DBT Star College Program, Electronics* to be held during **Oct 03 – 06, 2018.**

Dr. Poonam Kasturi, *Convener-Workshop /*
Dr. Manoj Saxena, *Coordinator-DBT Star College Program*
Deen Dayal Upadhyaya College, University of Delhi, New Delhi

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Program Schedule

DAY 1: Oct 03, 2018	**Wednesday**
09:00 am – 09:15 am	**Registration**
09.15 am – 09.30 am	**Inauguration**
09:30 am – 10:30 am	Introduction to VHDL
10:30 am – 10:45 am	***Tea Break***
10:45 am – 11:45 am	Data Flow Modeling – Combinational Circuits
11:45 am – 12:45 pm	Xilinx ISE Tool Flow with FPGA based coding technique
12:45 pm – 01:30 pm	***Lunch Break***
01.30 pm – 04:30 pm	**LAB SESSION**
	Lab 1: Simulation of Combinational Circuits - gates, half adder, half subtractor, 4x1 multiplexer, etc.
	Lab 2: Create Test Bench for the combinational circuits
	Tea Break
	Lab 3: Synthesize codes for combinational circuits on FPGA
DAY 2 : Oct 04, 2018	**THURSDAY**
09:30 am – 10:30 am	Structural Modeling – Combinational Circuits
10:30 am – 10:45 am	***Tea Break***
10:45 am – 11:45 am	State Machines
11:45 am – 12:45 pm	Behavioral Modeling – Sequential Circuits
12:45 pm – 01:30 pm	***Lunch Break***
01.30 pm – 04:30 pm	**LAB SESSION**
	Lab 4: Simulation of Combinational Circuits through structural modeling techniques - full adder, full subtractor, 4-bit binary parallel adder, 16 x 1 multiplexer, etc.
	Lab 5: Test Bench Simulation of sequential circuits – Flip Flops, Counters and Registers
	Tea Break
	Lab 6: Synthesizing sequential circuits, counters, on FPGA

Resource Persons

Dr. Poonam Kasturi, Associate Professor, Department of Electronics
Deen Dayal Upadhyaya College, University of Delhi
Dr. Manoj Saxena, Associate Professor, Department of Electronics
Deen Dayal Upadhyaya College, University of Delhi

For Hands-on-Session

Ms. Neha Malik, Assistant Professor, Department of Electronics, Deen Dayal Upadhyaya College, DU
Mr. Naveen Kumar, Assistant Professor, Department of Electronics, Deen Dayal Upadhyaya College, DU
Mr. Ajit Singh, Assistant Professor, Department of Electronics, Deen Dayal Upadhyaya College, DU

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DAY 3: Oct 05, 2018	**FRIDAY**
09:30 am – 10:30 am	FPGA Architecture – 7 Series
10:30 am – 10:45 am	***Tea Break***
10:45 am – 11:45 am	Overview of Xilinx Vivado tool targeting seven series FPGA.
11:45 am – 12:45 pm	Xilinx Vivado Tool Flow with FPGA based coding techniques
12:45 pm – 01:30 pm	***Lunch Break***
01.30 pm – 04:30 pm	**LAB SESSION**
	Lab 7: Implement on FPGA combinational design using Xilinx Vivado Tool
	Lab 8: Implement on FPGA sequential design using Xilinx Vivado Tool
	Tea Break
	Lab 9: Xilinx Design Constraints
	Create a project with I/O Planning type, enter pin locations, and export it to the RTL.

DAY 4 : Oct 06, 2018	**SATURDAY**
09:30 am – 10:30 am	Simple Hardware Design Create a Vivado project and use IP Integrator to develop a basic embedded system for a target board.
10:30 am – 10:45 am	***Tea Break***
10:45 am – 11:45 am	Adding Peripherals in Programmable Logic
11:45 am – 12:45 pm	Extend the hardware system by adding AXI peripherals from the IP catalog.
12:45 pm – 01:30 pm	***Lunch Break***
01.30 pm – 04:30 pm	**LAB SESSION**
	Lab 10: Debugging using Vivado Logic Analyzer cores : Insert various Vivado Logic Analyzer cores to debug/analyze system behavior
	Lab 11: Simple Hardware Design
	Create a Vivado project and use vio core to perform logic analysis .
	Tea Break
	Lab 12: Debugging using Logic Analyzer Tool Lab
	Explain Xilinx design constraint and how to use it in design using Vivado.
	Analyze the real time waveform using Chipscope-Pro analyzer
4.30pm – 5.00pm	**Interactive Q&A Session Followed by Valedictory session**

Resource Persons

Mr. Mayank Singh

Application Engineer, CoreEL Technologies Pvt. Ltd., Xilinx University Program (XUP)